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10/679,000	10/02/2003	Robert C. Chang	SANDP039	8920

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ANDERSON, LEVINE & LINTEL L.L.P.
14785 PRESTON ROAD
SUITE 650
DALLAS, TX 75254

EXAMINER	
TSAI, SHENG JEN	
ART UNIT	**PAPER NUMBER**
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/679,000	CHANG ET AL.	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25 and 27-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/08/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicant's Amendments and Remarks filed on June 8, 2006 regarding application 10,679,000 filed on October 2, 2003.

2. Claims 1, 4, 7-8, 11, 15-16, 18-19, 23 and 28-29 have been amended.

Claim 26 has been cancelled.

Claims 1-25 and 17-31 are pending for consideration.

3. ***Response to Amendments and Remarks***

Applicant's amendments and remarks have been fully and carefully considered.

Independent claims 1, 11 and 23 each has been amended with the new, additional limitation of "encode the first segment according to a first ECC algorithm and encode the second segment according to a second ECC algorithm."

In response, a new ground of claim analysis based on a newly identified reference (Smith, US 6, 961,890) in combination of previously cited references has been embarked. Refer to the corresponding sections of the claim analysis for details.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA

1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-4, 6-7, 10-15, 17-18, 21-25, 27-28 and 31 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 21-27 and 36-46 of copending Application No. **10/678,893**, as shown in the following table. Although not all of the conflicting claims are exactly identical, they are extremely similar and are not patentably distinct from each other.

10/679,000	**10/678,893**
1. (currently amended) A method for encoding data associated with a page within a non-volatile memory of a memory system, the page having a data area and an overhead area, the method comprising: dividing at least a part of the page into at least two segments of the data, the at least two segments of the data including a first segment and a second segment; performing error correction code (ECC) calculations on the first segment according to a first ECC algorithm to encode the first segment; and performing the ECC calculations on the second segment according to a second ECC algorithm to encode the second segment, wherein the second segment is encoded	36. A memory system comprising: a non-volatile memory including a plurality of blocks, the blocks including a first block and a second block, the first block including a first set of contents encoded using a first algorithm, the second block including a second set of contents encoded using a second algorithm, wherein the non-volatile memory further includes a data structure that is arranged to indicate that the first set of contents is encoded using the first algorithm and that the second set of contents is encoded using the second algorithm; code devices for accessing the data structure, wherein the code devices for accessing the data structure include code devices for determining that the first set of contents is encoded using the first

substantially separately from the first segment.	algorithm and code devices for determining that the second set of contents is encoded using the second algorithm; and a memory area that stores the code devices.
2. The method of claim 1 wherein the first segment includes the data area and the second segment includes the overhead area.	37. The memory system of claim 36 wherein the first algorithm is a 1-bit ECC algorithm and the second algorithm is a 2-bit ECC algorithm.
3. The method of claim 1 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.	38. The memory system of claim 37 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.
4. The method of claim 1 wherein the first ECC calculations are associated with an ECC algorithm that is arranged to detect up to two incorrect bits and to correct up to one of the incorrect bits in each of the first segment and the second segment.	39. A memory system comprising: a non-volatile memory that includes a first block into which data is to be stored; means that identify the first block; means that obtain an indicator associated with the first block; means that determine when the indicator indicates that the data is to be encoded using a first algorithm; and means that encode the data using the first algorithm when it is determined that the data is to be encoded using the first algorithm.
5. The method of claim 4 wherein the first ECC algorithm is a Hamming Code ECC algorithm.	40. The memory system of claim 39 further including: means that encode the data using a second algorithm when it is determined that the data is not to be encoded using the first algorithm; and means that write the data encoded using the second algorithm into the first block.
6. The method of claim 1 wherein dividing the at least part of the page into the at least two segments of the data includes: dividing the page into three segments, the three segments including the first segment, the second segment, and a third segment.	41. The memory system of claim 40 wherein the first algorithm is a 1-bit ECC algorithm and the second algorithm is a 2-bit ECC algorithm.
7. The method of claim 6 further including: performing the ECC calculations on the third segment to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment.	42. The memory system of claim 39 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.
8. The method of claim 6 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes the overhead area.	43. A memory system comprising: a non-volatile memory that includes a first block from which data is to be read; means that identify the first block; means that obtain an indicator associated with the first block; means that determine when the

	indicator indicates that the data stored in the first block has encoded using a first algorithm; and means that decode the data using the first algorithm when it is determined that the data has been encoded using the first algorithm.
9. The method of claim 6 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.	44. The memory system of claim 43 further including: means that decode the data using a second algorithm when it is determined that the data has not been encoded using the first algorithm.
10. The method of claim 1 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.	45. The memory system of claim 44 wherein the first algorithm is a 1-bit ECC algorithm and the second algorithm is a 2-bit ECC algorithm.
11. A memory system comprising: a non-volatile memory, the non-volatile memory including a page, the page having a data area and an overhead area, the data area and the overhead area being arranged to contain bits of data; code devices for dividing at least a part of the page into at least two segments, the at least two segments including a first segment and a second segment; code devices for performing error correction code (ECC) calculations on the first segment according to a first ECC algorithm to encode the first segment and on the second segment according to a second ECC algorithm to encode the second segment, wherein the second segment is encoded substantially separately from the first segment; and a memory area for storing the code devices.	46. The memory system of claim 43 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.
12. The memory system of claim 11 further including: a controller, the controller being arranged to process the code devices.	21. A memory system comprising: a non-volatile memory including a plurality of blocks, the plurality of blocks including a first block; code devices for identifying the first block into which data is to be stored; code devices for obtaining an indicator associated with the first block; code devices for determining when the indicator indicates that the data is to be encoded using a first algorithm; code devices for encoding the data using the first algorithm when it is determined that the data is to be encoded using the first algorithm; code devices for writing the data encoded using the first algorithm into the first block; and a memory area that stores the code devices.
13. The memory system of claim 11	22. The memory system of claim 21 further

wherein the first segment includes the data area and the second segment includes the overhead area.	including: code devices for encoding the data using a second algorithm when it is determined that the data is not to be encoded using the first algorithm; and code devices for writing the data encoded using the second algorithm into the first block.
14. The memory system of claim 11 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.	23. The memory system of claim 22 wherein the first algorithm is a 1-bit ECC algorithm and the second algorithm is a 2-bit ECC algorithm.
15. The memory system of claim 11 wherein the first ECC calculations are associated with an ECC algorithm that is arranged to detect up to two incorrect bits and to correct up to one of the incorrect bits in each of the first segment and the second segment.	24. The memory system of claim 22 wherein the indicator is arranged to indicate when the block is a reclaimed block, wherein when the block is a reclaimed block, the indicator is further arranged to indicate that the data is to be encoded using the second algorithm.
16. The memory system of claim 15 wherein the first ECC algorithm is a Hamming Code ECC algorithm.	25. The memory system of claim 22 wherein the indicator is arranged to indicate a number of times the block has been erased.
17. The memory system of claim 11 wherein the code devices for dividing the at least part of the page into the at least two segments include: code devices for dividing the page into three segments, the three segments including the first segment, the second segment, and a third segment.	26. The memory system of claim 25 wherein the code devices for determining when the indicator indicates that the data is to be encoded using the first algorithm include: code devices for determining when the indicator is less than a threshold value, wherein when the indicator is less than the threshold value, the data is to be encoded using the first algorithm.
18. The memory system of claim 17 further including: code devices for performing the ECC calculations on the third segment according to one of the first and second ECC algorithm to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment.	27. The memory system of claim 21 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.
19. The memory system of claim 17 wherein the first segment includes a first section of the data area, the third segment includes a second section of the data area, and the second segment includes the overhead area.	
20. The memory system of claim 17 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the	

third segment includes a third section of the data area.	
21. The memory system of claim 11 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.	
22. The memory system of claim 11 wherein the code devices are one of software code devices and firmware code devices.	
23. A memory system comprising: a non-volatile memory, the non-volatile memory including a page, the page having a data area and an overhead area, the data area and the overhead area being arranged to contain bits of data; means that divide at least a part of the page into at least two segments, the at least two segments including a first segment and a second segment; and means that perform error correction code (ECC) calculations on the first segment according to a first ECC algorithm to encode the first segment and on the second segment according to a second ECC algorithm to encode the second segment, wherein the second segment is encoded substantially separately from the first segment.	
24. The memory system of claim 23 wherein the first segment includes the data area and the second segment includes the overhead area.	
25. The memory system of claim 23 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.	
27. The memory system of claim 23 wherein the means that divide the at least part of the page into the at least two segments include: means that divide the page into three segments, the three segments including the first segment, the second segment, and a third segment.	
28. The memory system of claim 27 further including: means that perform the ECC calculations according to one of the first and second ECC algorithms on the third segment to encode the	

third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment.	
29. The memory system of claim 27 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes the overhead area.	
30. The memory system of claim 27 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.	
31. The memory system of claim 23 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.	

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-3, 6-9, 11-14, 17-20, 22-25 and 27-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Smith (US 6,961,890).

As to claim 1, Smith discloses **a method for encoding data associated with a page within a non-volatile memory of a memory system** [Dynamic Variable-Length Error Correction Code (title; abstract)], the page having a data area and an overhead area, the method comprising:

dividing at least a part of the page into at least two segments of the data, the at least two segments of the data including a first segment and a second segment [a divider segregating the payload and redundancy portions may be dynamically relocated, thereby altering the size of the redundancy to allow for use of an error correcting code selected to provide the data integrity required in response to changing conditions (abstract); figures 1 and 2 show the dividing of a memory page into a plurality of segments (206, 208, 210 and 212); column 4, lines 16-31];

performing error correction code (ECC) calculations on the first segment according to a first ECC algorithm to encode the first segment [The fundamental error rate is particularly dependent upon factors that are a function of time. For example, the fundamental error rate of memory devices based on some technologies may increase over time in response to degradation of an insulation layer. Accordingly, a level of redundancy that is appropriate for the fundamental error rate at the date of manufacture could be inadequate after a period of time. However, a level of redundancy that is appropriate at some date in the future might be excessive during the period of time the device was most likely to be used, immediately following manufacture (column 1, lines 45-55); Accordingly, it would be beneficial to develop a variable-length error correction code and method of use that dynamically alters the redundancy

available to allow substitution of a first ECC with a second ECC in response to changing error rates, and which allows more efficient allocation of memory between payload and redundancy (column 2, lines 6-11); column 3, lines 28-36]; **and**

performing error correction code (ECC) calculations on the second segment according to a second ECC algorithm to encode the second segment [The fundamental error rate is particularly dependent upon factors that are a function of time. For example, the fundamental error rate of memory devices based on some technologies may increase over time in response to degradation of an insulation layer. Accordingly, a level of redundancy that is appropriate for the fundamental error rate at the date of manufacture could be inadequate after a period of time. However, a level of redundancy that is appropriate at some date in the future might be excessive during the period of time the device was most likely to be used, immediately following manufacture (column 1, lines 45-55); Accordingly, it would be beneficial to develop a variable-length error correction code and method of use that dynamically alters the redundancy available to allow substitution of a first ECC with a second ECC in response to changing error rates, and which allows more efficient allocation of memory between payload and redundancy (column 2, lines 6-11); column 3, lines 28-36], **wherein the second segment is encoded substantially separately from the first segment** [figure 2, column 4, lines 16-31].

As to claim 2, Smith teaches that **the first segment includes the data area** [the payload portion (figure 2, 202)] **and the second segment includes the overhead area** [the redundancy portion (figure 2, 204)].

As to claim 3, Smith teaches that **the first segment includes a first section of the data area** [figure 2, 210] **and the second segment includes a second section of the data area** [figure 2, 208].

As to claim 6, Smith teaches that **dividing the at least part of the page into the at least two segments of the data includes**:
dividing the page into three segments, the three segments including the first segment, the second segment, and a third segment [a divider segregating the payload and redundancy portions may be dynamically relocated, thereby altering the size of the redundancy to allow for use of an error correcting code selected to provide the data integrity required in response to changing conditions (abstract); figures 1 and 2 show the dividing of a memory page into a plurality of segments (206, 208, 210 and 212); column 4, lines 16-31].

As to claim 7, Smith teaches that **performing the ECC calculations on the third segment according to one of the first and second ECC algorithms to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment** [The fundamental error rate is particularly dependent upon factors that are a function of time. For example, the fundamental error rate of memory devices based on some technologies may increase over time in response to degradation of an insulation layer. Accordingly, a level of redundancy that is appropriate for the fundamental error rate at the date of manufacture could be inadequate after a period of time. However, a level of redundancy that is appropriate at some date in the future might be excessive during the period of time the

device was most likely to be used, immediately following manufacture (column 1, lines 45-55); Accordingly, it would be beneficial to develop a variable-length error correction code and method of use that dynamically alters the redundancy available to allow substitution of a first ECC with a second ECC in response to changing error rates, and which allows more efficient allocation of memory between payload and redundancy (column 2, lines 6-11); column 3, lines 28-36].

As to claim 8, Smith teaches that **the first segment includes a first section of the data area** [figure 2, 212]**, the third segment includes a second section of the data area** [figure 2, 210]**, and the second segment includes the overhead area** [figure 2, 214].

As to claim 9, Smith teaches that **the first segment includes a first section of the data area** [figure 2, 212]**, the second segment includes a second section of the data area** [figure 2, 210]**, and the third segment includes a third section of the data area** [figure 2, 208].

As to claim 11, refer to "As to claim 1."

As to claim 12, Smith teaches that **the memory system of claim 11 further including: a controller, the controller being arranged to process the code devices** [An application determination module 506 is adapted to determine the use to which the storage device 201 is to be put (column 6. lines 59-65); A code assignment module 508 is adapted to select an appropriate ECC from among those available in the ECC library 510, and also to select a level of redundancy required to accommodate information according to the code selected (column 7, lines 10-15); An error tracking,

analysis and recording module 602 collects and records errors in the storage media (column 7, lines 45-47); A self-test module 604 provides a memory test that can thoroughly test the storage device 201 (column 7, lines 49-50); An age and use-tracking module 606 calculates the chronological age of the storage device 201 and the number of uses (column 7, lines 51-53); A storage application-tracking module 608 interfaces with the device or system within which the storage device 201 is installed, thereby allowing it to determine the use to which the storage device is being put (column 7, lines 57-59); the controller comprises all these modules].

As to claim 13, refer to "As to claim 2."

As to claim 14, refer to "As to claim 3."

As to claim 17, refer to "As to claim 6."

As to claim 18, refer to "As to claim 7."

As to claim 19, refer to "As to claim 8."

As to claim 20, refer to "As to claim 9."

As to claim 22, Smith teaches that **the code devices are one of software code devices and firmware code devices** [figure 7 shows the software procedure for calculating the ECC code for each page].

As to claim 23, refer to "As to claim 1."

As to claim 24, refer to "As to claim 2."

As to claim 25, refer to "As to claim 3."

As to claim 27, refer to "As to claim 6."

As to claim 28, refer to "As to claim 7."

As to claim 29, refer to "As to claim 8."

As to claim 30, refer to "As to claim 9."

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 4-5, 15-16, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith (US 6,961,890), and in view of Zhang et al. (US 6,662,333).

As to claim 4, Smith does not explicitly mention that **the first ECC calculations are associated with an ECC algorithm is arranged to detect up to two incorrect bits and to correct up to one of the incorrect bits in each of the first segment and the second segment.**

However, Smith does teach that the ECC library 510 typically contains a plurality of ECCs, including at least one weaker parity type code 512, at least one stronger BCH code 514, and at least one very strong Reed Solomon codes 516. To apply one of these ECCs to the redundancy 204 associated with the data structure 200, an appropriate divider similar to divider 206 may be selected to result in the required division between the payload and redundancy in the data structure 200 (column 7, lines 22-29).

Further, Applicants admit in the Background of the Invention Section of their disclosure that the above recited feature is well known in the art [some ECC algorithms

that are used to encode and decode data for storage are known as 1-bit ECC algorithms and 2-bit ECC algorithms ... (paragraph 0009)].

Moreover, Zhang et al. disclose in their invention "Shared Error Correction for Memory Design" an ECC scheme in which single bit errors are corrected and double bit errors are detected [column 1, lines 24-33].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the particular limitation recited in this claim is well known in the art, as demonstrated by Applicants' admission as well as Zhang et al., hence lacking patentable significance.

As to claim 5, Smith does not explicitly mention that **the ECC Algorithm is a Hamming Code ECC Algorithm**.

However, Smith does teach that the ECC library 510 typically contains a plurality of ECCs, including at least one weaker parity type code 512, at least one stronger BCH code 514, and at least one very strong Reed Solomon codes 516. To apply one of these ECCs to the redundancy 204 associated with the data structure 200, an appropriate divider similar to divider 206 may be selected to result in the required division between the payload and redundancy in the data structure 200 (column 7, lines 22-29).

Further, Zhang et al. teach in their invention "Shared Error Correction for Memory Design" that Hamming Code based ECC algorithms are well known in the art [a well known error correction code is the Hamming code (column 1, lines 55-67)].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the particular limitation recited in this claim is well known in the art, as demonstrated Zhang et al., hence lacking patentable significance.

As to claim 15, refer to "As to claim 4."

As to claim 16, refer to "As to claim 5."

As to claim 26, refer to "As to claims 4-5."

10. Claims 10, 21 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith (US 6,961,890), and in view of Kramer (US 6,182,239).

As to claims 10, 21 and 31, Smith does not mention that **the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.**

However, the inventions of Smith are directly applicable to any type of flash memories, including NAND flash memory and MLC NAND flash memory.

Further, Kramer teaches in the invention "Fault-Tolerant Codes for Multi-Level Memories" a fault-tolerant code semiconductor flash memory storage devices including an array of individual multi-level cell (MLC) storage devices [abstract; column 2, lines 1-15] as well as NAND flash memory [column 2, lines 36-57].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the particular limitation recited in this claim is well known in the art, as demonstrated Kramer, hence lacking patentable significance.

11. ***Related Prior Art On Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Carnevale et al., (US 6,353,910), "Method and Apparatus for Implementing Error Correction Coding (ECC) in a Dynamic Random Access Memory Utilizing Vertical ECC Storage."
- Payne et al., (US 2003/0099140), "Data Handling System."
- Benton et al., (US 5,164,944), "Method and Apparatus for Effecting Multiple Error Correction in a Computer Memory."
- Sinclair et al., (US Patent Application Publication 2003/0156473), "Memory Controller."
- Moro et al., (US 6,769,087), "Data Storage Device and Method for Controlling the Device."
- Purdham, (US 5,666,371), "Method and Apparatus for detecting Errors in a System that Employs Multi-Bit Wide Memory Elements."
- Kellogg et al., (US 5,896,404), "Programmable Burst Length DRAM."

Conclusion

12. Claims 1-25 and 27-31 are rejected as explained above.

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

June 19, 2006

PIERRE BATAILLE
PRIMARY EXAMINER
6/20/06